REMARKS/ARGUMENTS

In a Final Office Action dated October 18, 2006 claims 1-36 were rejected under § 103 over Edsall and Testardi. Applicants respectfully traverse the § 103 rejections and request consideration of the following arguments.

§ 103 Rejections

Applicants respectfully submit that the present claims are allowable.

Claim 19

Claim 19 is being treated as an exemplary claim in these remarks to better track the Office Action. The Office Action rejected claim 19 over Edsall and Testardi. Applicants respectfully traverse the rejection.

The Final Office Action provided comments addressing Applicants prior remarks and revised the rejection to correspond to those comments. Applicants submit that the claim is patentable even given the comments and new rejection.

The new rejection apparently somehow combines the basic data transfer capabilities of Edsall (connectors 302 and 204, MAC 304 and 322 and switches 306 and 320) and the fast path of Testardi, though how the two are combined is not stated. In fact, the Office Action defines the I/O modules to be the fast path of Testardi without any reference to Edsall. The Edsall pieces do not include the required processors in the I/O module, with the Testardi fast path apparently filling this requirement.

Applicants note that the claim specifically requires that the storage processing device may have the storage units directly connected or coupled through an external switch and the data migration is performed in either case. Applicants submit that the combination of Edsall and Testardi do not teach or suggest this requirement. The switches 306 and 320 of Edsall have been corresponded to being part of the I/O module, not the external switch required by the claims. Testardi is apparently cited for the

processing in the I/O module as well as the control module with the required interactivity. However Testardi does not teach or suggest that the storage devices can be connected through a switch and have the processing of Testardi still be operational. Testardi indicates that the storage units must be directly connected to the storage processing device. Figure 4A of Testardi shows direct connection but at a general level. Figure 4B of Testardi is more specific and shows the hosts and storage units directly connected. Figure 4C adds external switches to Figure 4B but only hosts are attached to the switches, not storage units. There is no teaching or suggestion in Testardi that the storage units can be connected to the storage processing device through a switch and have the data migration operations still be successfully performed. While Edsall may show storage units connected to switches, this does not overcome the limitations of Testardi in this regard as the elements being used in Edsall do not contain any of the processing capabilities required in the claim and those processing capabilities are limited to directly connected storage units. Asserting that the storage units could be connected through a switch goes against the express teachings of Testardi and so would be an improper rejection.

Applicants thus submit that the combination of Edsall and Testardi, even as combined in the new rejection, do not teach or suggest all of the required claim elements.

Because this required element of claim 19, and similar claims 1, 10 and 28, is missing, Applicants submit that all of the present claims are allowable.

Claim 21

As an exemplary claim, Applicants will address the rejection of claim 21. The Office Action stated that Testardi discloses the fast path delaying data write operations if the barrier entry relates to data write operation by faulting the operations to the control path. The Office Action then notes that this is interpreted as the fast path delaying the write operations on the barrier range. Applicants respectfully traverse this interpretation. The claim requires the processors, which are located in the input/output module, to delay

the write operations. The cited operation of Testardi has the fast path, equated to the processors of the claim, not handling the operation at all but transferring the operation to the control path, which then faults the operation to force a retry. But the claim requires the processors, i.e. the fast path, delaying the operation. In Testardi the fast path does nothing, not delay, not handle, nothing. It simply passes the operation on to the control path. This does not meet the positive requirement in the claim that the processors perform the delaying operation. Applicants understand and acknowledge the statement that the limitations of the specification are not to be read into the claims but submit that the requirement that the processors delay the write operation is a positive element in the claims and that the fast path of Testardi passing off the operation does not meet the positive requirement of the processors delaying the operation. There is no teaching or suggestion to have the fast path perform a delay rather than pass off the operation.

Applicants submit that claim 21 and similar claims 3, 8, 12, 17, 26, 30 and 35 are allowable.

CONCLUSION

Based on the above remarks Applicants respectfully submit that all of the present claims are allowable. Reconsideration is respectfully requested.

Respectfully submitted,

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